International Journal of Research in Engineering and Innovation (IJREI)
journal home page: http://www.ijrei.com
ISSN (Online): 2456-6934

Miniature power-efficient time-based differential analog-to-digital converters

Abdullah El-Bayoumi

Valeo InterBranch Automotive Software, Egypt

Abstract

Time-Based Analog-to-Digital Converter (ADC), at scaled CMOS technology, plays a major role in designing Software Defined Radio (SDR) receivers as it manifests higher speed and lower power than conventional ADCs. Time-Based ADC includes a Voltage-to-Time Converter (VTC) or a Voltage-Controlled Delay Unit (VCDU) which converts the input voltage into a pulse delay, and a Time-to-Digital Converter (TDC) which converts the pulse delay into a digital word. In this paper, we present two novel differential VTCs fabricated using TSMC 65nm CMOS technology with ideal TDCs and no sample-and-hold circuit producing complete ADCs. The first proposed ADC is based on the design of a VCDU. This new ADC operates on a higher sampling frequency of 8 Gsample/sec, with a supply voltage of 1-V. It achieves a wider dynamic-range of 560 mV and a 3% linearity error. Simulation results reveal that this design can achieve up to a 9-bit resolution with Effective Number of Bits (ENOB) of 8.9902 bits in an 8-GHz bandwidth and a 0.3918 fJ/conversion FOM. It consumes a 1.594 mW power. The second proposed ADC is based on a new design methodology which reports a wider dynamic range of 1 V and a higher sensitivity of 9.6 ps/mV. This new ADC operates on a 2.5 Gsample/sec sampling frequency with a 3% linearity error and with a supply voltage of 1.2 V. It also achieves a resolution up to 11 bits with ENOB of 10.7228 bits in a 2.5-GHz bandwidth and a 0.03763 fJ/conversion FOM. It consumes a 0.159 mW power.

Keywords: Nanometer CMOS technology, analog-to-digital converter, ADC, voltage-controlled delay unit, voltage-to-time converter, time-to-digital converter, software defined radio, ENOB.

1. Introduction

Nowadays, the effluence of scaling CMOS technology invades all industrial and scientific communities. This drift overcomes the main problem resulted from using conventional Analog-to-Digital Converters (ADCs) [1] in such applications. In fact, due to the capacity of demands, a single Integrated Circuit (IC) chip is intended to have several chains of transmitting and receiving blocks needed for different wireless standards which require from the ADC: a proper sampling frequency and a proper dynamic range. This produces much energy density of rechargeable power sources which does not increase as fast as the power consumption of the electronics, so increasing the source power is not the aimed solution.

This induces applications such as Software Defined Radio (SDR) receivers to arise [1], [2]. The SDR IC configures and controls the chain that we want to use, otherwise all chains will be switched on. In SDR receiver, the received noisy RF analog signal is directly applied to a wide-band ADC, followed by the real time Digital Signal Processor (DSP). New ADCs can be reconfigured according to the SDR standard. This leads us to think about new techniques of ADCs design with much small area and low power consumption.

In deep sub-micron CMOS technology, technology scaling makes the ADC design much more complex, as it reduces the supply voltage which results in degrading the headroom level of the signal (signal swing) and the signal-to-noise ratio (SNR). Besides, it has a little effect on the threshold voltage resulting in design complexity (i.e. difficulty in cascading which is the fundamental concept of the op-amp design) [3].

Corresponding author: Abdullah El-Bayoumi
Email Id: abdullah.elbayoumi@pg.cu.edu.eg

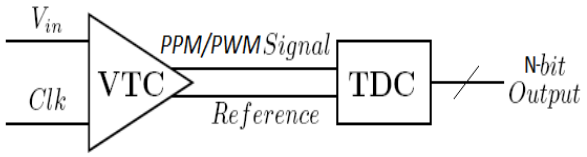

Fig. 1. Time-based ADC architecture.

With these causes, the conventional ADCs are not the promising solutions in lower technology nodes.

In high frequencies, the time resolution of digital signals is much greater than the voltage resolution of the analog signals, so we do not need an op-amp or an explicit sample and hold circuit in the Time-Based ADC design. Consequently, We will increase the percentage of the digital part of the system using digital CMOS technology in order to: solve analog design problems, get the full use of the digital signal processing, reduce area and power consumption, have faster ADCs with higher performance and make the ADC move more and more to the signal input.

In Time-Based ADC, the analog signal amplitude is sampled and converted into a pulse in time-domain by modulating edges of the reference signal, then the time-domain pulse is quantized into a digital output. This operation is done using a Voltage-to-Time Converter (VTC) and a Time-to-Digital Converter (TDC) respectively as shown in Fig. 1. The VTC is also referred to as either a Pulse Position Modulator (PPM) or Pulse Width Modulator (PWM), depending on whether the delay is applied to one or both edges of the input clock pulses [4]. The TDC circuit consists of digital logic and counter circuits [5].

Several VTC circuits have been introduced in the literature [4], [6]–[8]. The basic core in these circuits is the current starved inverter, in which the applied analog input voltage (V_{IN}) controls the fall time and makes the pulse width of the output inversely proportional to it. On the other hand, the basic Voltage-Controlled Delay Unit (VCDU) circuit proportionally controls the delay of the input clock edge with respect to a sampled input voltage. The designs of several VCDU circuits in CMOS 0.18μm technology have been shown in [9]. All previously published circuits are facing several limitations and design trade-offs between dynamic range, linearity and the ADC resolution. Also, they suffer from limited sensitivity.

There are significant advantages in the differential design. First, the common-mode noise will be rejected. Second, the differential input offers doubling of the signal amplitude resulting in a 6-dB improvement in the SNR. Finally, the even-order harmonic distortion components caused by a single-ended VTC circuit or the VCDU circuit non-linearity will be suppressed.

In this paper, we will focus on designing an ADC based on the VCDU in 65nm technology, and propose a new design based on the differential approach at first. Second, another new ADC circuit based on the differential architecture and a new design methodology is proposed. Finally, by gathering all advantages from the usage of lower technology nodes till these novels, we achieve promising results in linearity, dynamic range, sensitivity and resolution at reasonable expense of extra area/ power overheads.

The rest of the paper is organized as follows. In Section 2, the design and analysis of an ADC based on the VCDU circuit is discussed. In Section 3, the design and analysis of an ADC based on a new design methodology is discussed. Simulation results for both designs are illustrated in Section 4. Finally, a conclusion is summarized in Section 5.

2. ADC Based on a VCDU Design and Analysis

2.1 ADC Based on Voltage-Controlled Delay Unit

At first, we convert the input voltage into a delay using a VCDU circuit. The VCDU circuit has 2 inputs: a reference clock event (Φ_{CLK}), and the sampled V_{IN}. Fig. 2 shows the VCDU functional diagram, in which the direct voltage-controlled delay is generated by charging the capacitor. This is done using a constant current (I_{IN}), when Φ_{CLK} rising edge is high [10]. The comparator output switches to logic '1', once t-he capacitor voltage reaches the desired V_{IN}. Hence, the output time-difference (ΔT_O), as portrayed in Fig. 3, is the time inter-val between the comparator output switching time (Φ_O) and Φ_{CLK}. Equation (1) describes the conversion process that is done by the voltage-to-time conversion factor (G_Φ).

$$\Delta T_O(n) = \frac{C}{I_{IN}} V_{IN}(n) = G_\Phi V_{IN}(n) \qquad (1)$$

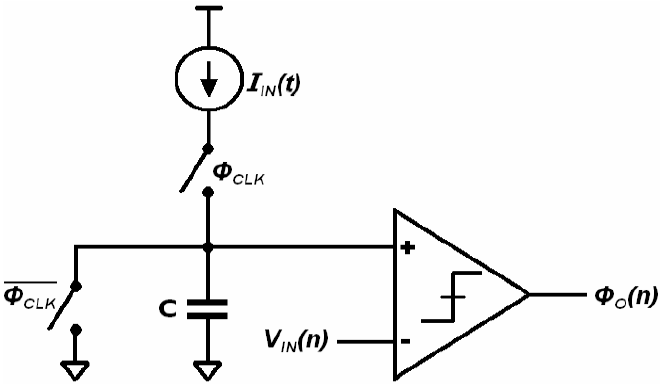

Fig. 2. VCDU functional diagram.

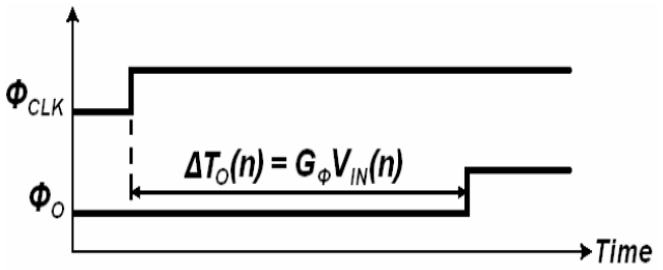

Fig. 3. VCDU Timing diagram.

Fig. 4 portrays the VCDU circuit schematic. It includes a Wilson current mirror [11] which is formed by transistors M1-M3, used to generate I_{IN}. M2 has a high gate voltage as an expense to decrease the high sensitivity of the current value to neglect gain-source voltage variations. During the logic '0' of Φ_{CLK}, the capacitor is reset via M6. When Φ_{CLK} raises up to logic '1', the capacitor charges through the transmission gate switch formed by M4 and M5. The current-steering amplifier, constructed by M7-M13, senses the difference between the input voltage V_{IN} and the capacitor voltage and permits the output latching circuit (M14-M17) to make a logic decision.

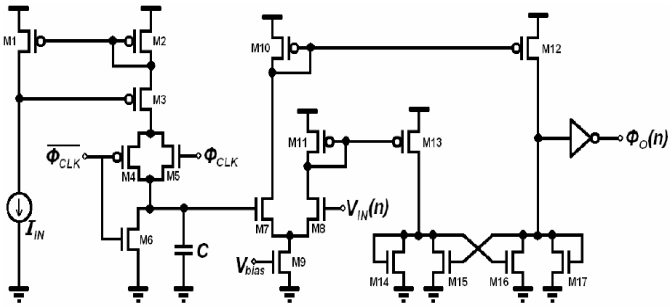

Fig. 4. The VCDU Circuit schematic.

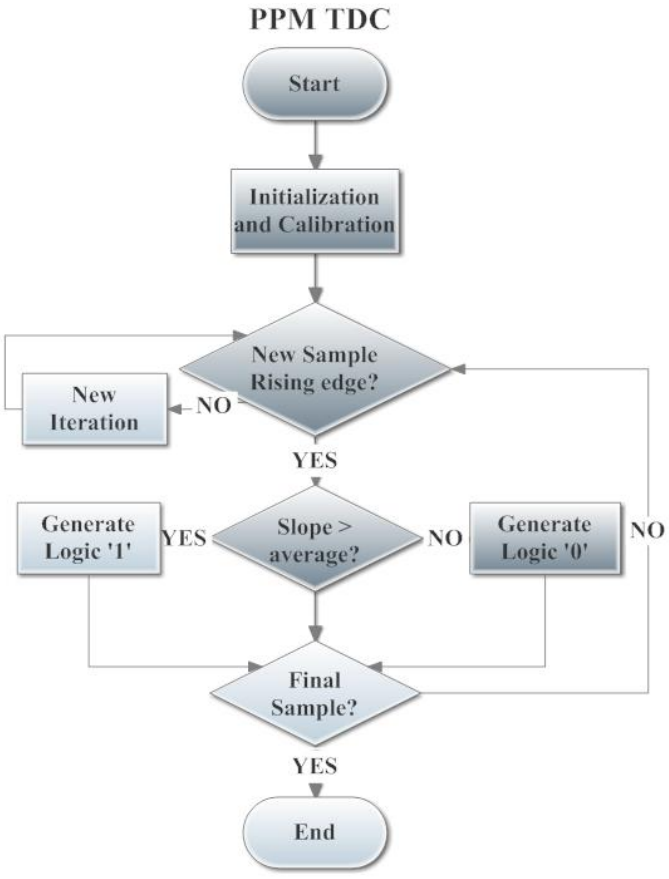

Fig. 5. Ideal TDC flowchart based on PPM using MATLAB.

The second step is to convert the resulted delay into digital words using a TDC. As the VTC/VCDU can be categorized according to their modulation techniques (PPM and PWM), the TDC should be categorized the same way. For a PPM VCDU, we have designed an ideal TDC on MATLAB. The TDC takes its input from the output of the VTC/VCDU circuit.

In a TDC code, as illustrated in the flowchart of Fig. 5, an initialization and calibration phase are needed for neglecting some of the VCDU output samples that may suffer from some signal sparks. We use the slope of the output sample VCDU for detecting whether the current sample represents a '1' logic or a '0' logic. This is because the behavior of the VCDU output signal depends on the PPM approach. So, each rising-edge slope of the VCDU output sample has the modulated input signal information.

2.2 The Proposed ADC Based on Voltage-to-Time Converter

The first proposed ADC architecture which depends on PPM approach, is based on a VTC circuit. First, this VTC consists of a differential VCDU (i.e. the applied input voltage for each VCDU core equals $+V_{IN}/2$ and $-V_{IN}/2$, respectively) as shown in Fig. 6. Hence, we are able to convert voltage data into time-difference variables.

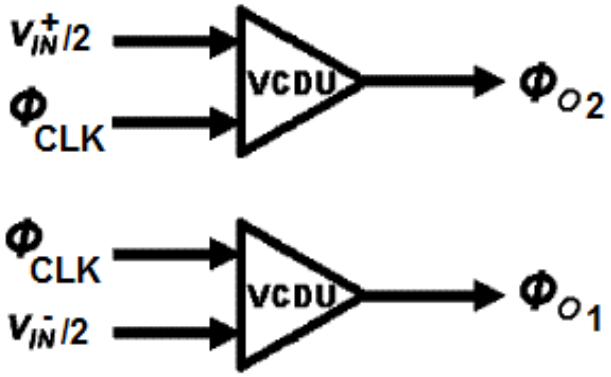

Fig. 6. VTC The first proposed architecture.

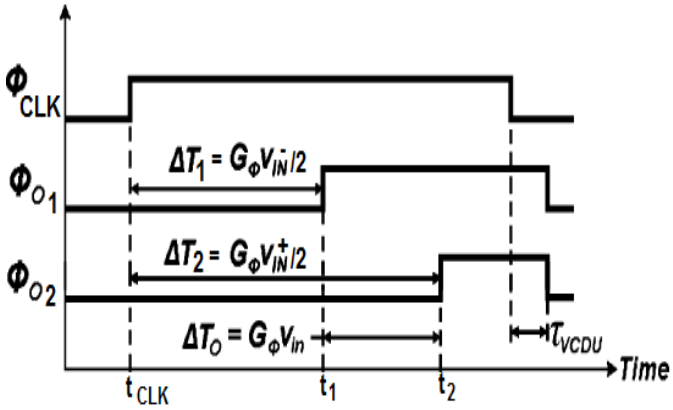

Fig. 7. VTC Timing diagram

The top VCDU core converts the positive difference between ΔT_2 and ΔT_1. Second, we will produce $V_{IN}/2$ into a time-difference variable (ΔT_2) which is measured with respect to Φ_{CLK}, while the other core converts the negative $V_{IN}/2$ into a time-difference variable (ΔT_1) which is measured with respect to Φ_{CLK}. As illustrated in Fig. 7, the resultant delay (ΔT_O) of the proposed design is the time- difference between $\Delta T2$ and $\Delta T1$. Second, we will produce digital outputs based on the same approach of a PPM TDC as illustrated in Fig. 5.

3. ADC Based on a New Methodology Design an and Analysis

In this paper, there are 3 new differential designs of current-starved VTC circuits. The first design intends to control the output falling edge of a PPM VTC. The second design intends to control the output rising edge of a PPM VTC. The final design integrated with a TDC block is the second proposed ADC architecture, in which all edges are modulated resulting in a PWM ADC. For a differential design, the applied input voltage for each VTC core equals $+V_{IN}/2$ and $-V_{IN}/2$. The mode of operation and the single ended design have been discussed in [7]. Fig. 8 shows the block diagram of a differential architecture that is used for all designs.

To get the delay equation of the 1st falling-differential VTC design, we should calculate at first the delay difference between the output falling edge and the clock rising edge for each core. Then, we get the difference (fall delay) between them. The same procedure to get the rise delay for the 2nd rising-differential VTC design is done, but we will calculate the delay difference between the output rising edge and the clock falling edge for each design core. For the final design, the delay equation is the difference between each core pulse-width. This is because it is based on PWM.

Fig. 9(a) represents the first part of a single-ended core for second proposed design which is the same as the basic current starved VTC circuit with a quite modification which is revealed as Na1 transistor. This transistor is used to add another path to flowing current, in case of lower values of $V_{IN}/2$. Its width should be much smaller than Na2 transistor, so it will have a higher resistance. This makes the current flow easier through Na2 which has a higher size. Same procedure is done for the second part of the single-ended core which is portrayed in Fig. 9(b) where the width of Pb2 is bigger than Pb3.

The idea of the proposed differential ADC, as the core [7] of its VTC shown in Fig. 10, is to have a maximum dynamic

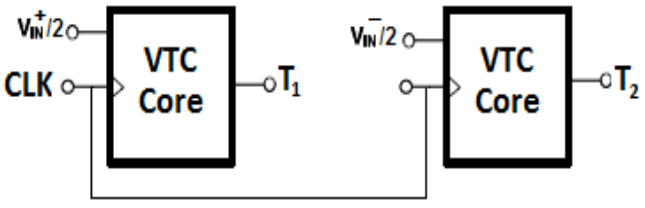

Fig. 8. The differential architecture of the falling VTC, rising VTC and the second proposed ADC.

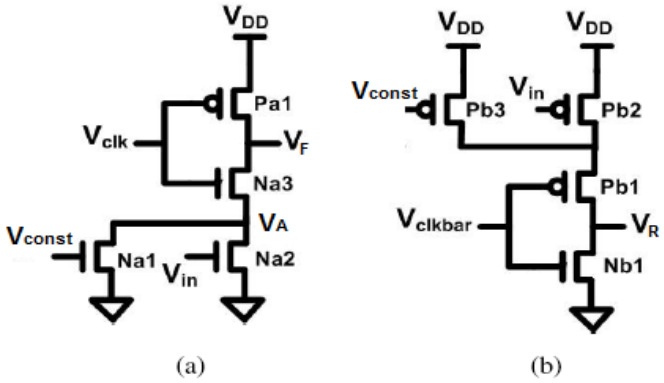

Fig. 9. Circuit schematic of Single-ended current-starved VTCs. (a) Rising circuit. (b) Falling circuit.

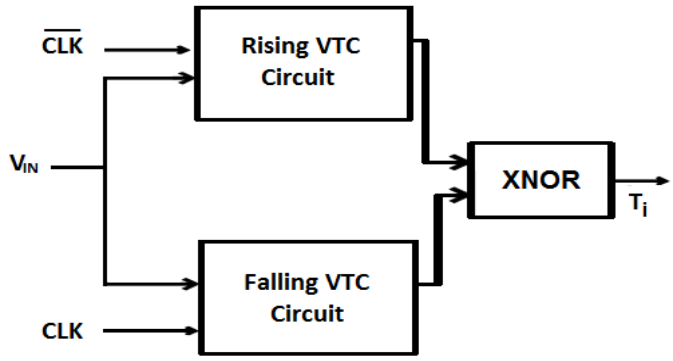

Fig. 10. The VTC core of the second proposed architecture.

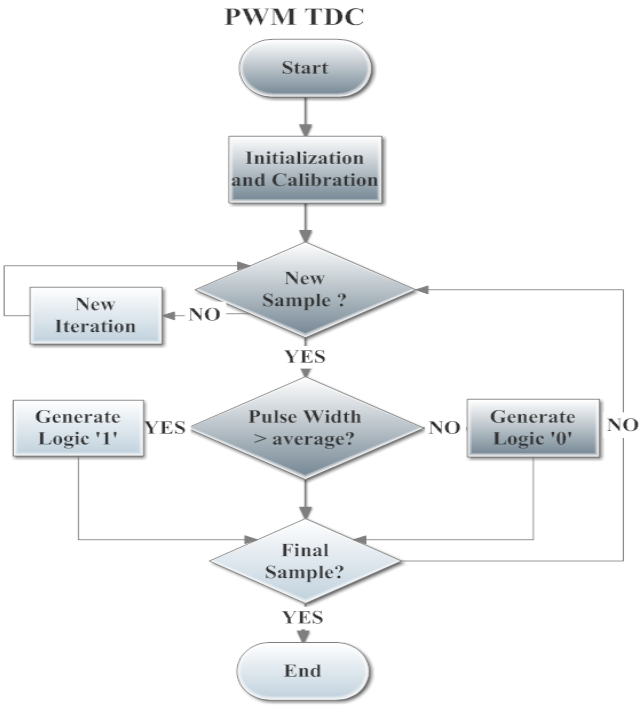

Fig. 11. Ideal TDC flowchart based on PWM using MATLAB.

range. This design is based on the complementary behavior between the pull-down network and the pull-up network of a single-ended VTC circuit. It has an inverted delayed clock using larger number of inverter-based delay elements for the pull-up network. This delay helps in having better resolution for low values of the output pulse which equals $\Delta + T_R - T_F$, where Δ is the buffer delay, T_R is the rise delay of the 2nd rising-differential VTC design, and T_F is the fall delay of the 1st falling-differential VTC design. The XNOR gate is responsible of getting the difference between T_R and T_F.

The following stage of the proposed VTC design is the TDC block. It depends on the PWM approach. A flowchart of how this TDC works is portrayed in Fig. 11. The first step is an initialization and calibration stage for providing stable samples. Then, we enter a comparison stage in which we generate a logic '1', if we have a new pulse-width greater than a specific average number. Otherwise, we have a logic '0'. This will be repeated till the final sample.

4. Simulation Results

Design simulations were carried out, by sweeping the input voltage, on Cadence Virtuoso using industrial hardware-calibrated Taiwan Semiconductor Manufacturing Corporation (TSMC) 65nm CMOS technology and the results were tested using MATLAB. For the single-ended ADC based on VCDU and the first proposed ADC, the supply voltage of both designs is 1 V. The applied DC input voltage is 546.5mV and 500 *m*V for each design, respectively. These values are the average numbers of the input voltage linear range. The operating clock frequency is 8 GHz for both designs. On the other hand, for the falling-differential VTC, the rising-differential VTC and the second proposed ADC; the supply voltage of the 3 designs of the new methodology is 1.2 V, the applied DC input voltage is 600 *m*V and the operating clock frequency is 250 MHz.

For the ADC based on the VCDU circuit, the first proposed ADC and the second proposed ADC; the average number used as a comparator in the TDC part is 1.8×10^{9} *p*s/*m*V, 4×10^{9} *p*s/*m*V and 0.04×10^{-9} *n*s respectively. There is a 11-cell buffer for a suitable output width used in the second proposed design.

4.1 Voltage Sensitivity and Linearity

To have a linearity error of 3%, we will sweep the input voltage, V_{IN}, for all designs and we will search for the linear range (dynamic range) that achieves this value in the delay-vs-VIN waveform. After estimating a linear line from the waveform, we will test the linearity on MATLAB. After some iterations, we will reach the 3% acceptable error. The linearity error check is based on curve fitting method, in which we get the difference between the fundamental coefficients of the actual linear equation that are produced from the schematic design on Cadence and the ideal first-order fundamental coefficients that fit the actual ones. In the linear range, we will choose any 2 points, and calculate the slope between the delay on y-axis and V_{IN} on x-axis to calculate the circuit sensitivity.

Table 1: ADC Based on VCDU Specifications

V_{IN} Range (*m*V)	-187 : +187
DR (*m*V)	374
Input DC Bias (*m*V)	546.5
Linearity Error (%)	3
Sensitivity (*p*s/*m*V)	0.29
F_S (GHz)	8
Power Dissipation (*m*W)	880
FOM_1 ($\times10^{12}$)	1.27

Table 2: The First Proposed ADC specifications

Property	Specifications at a 1GHz FS	Specifications at a 8GHz FS
V_{IN} Range (*m*V)	-535 : +535	-280 : +280
DR (*m*V)	1070	560
Input DC Bias (*m*V)	500	500
Linearity Error (%)	3	3
Sensitivity (*p*s/*m*V)	0.14	0.91
Power Dissipation (*m*W)	1.366	1.594
FOM_1 ($\times10^{12}$)	0.84	1.57

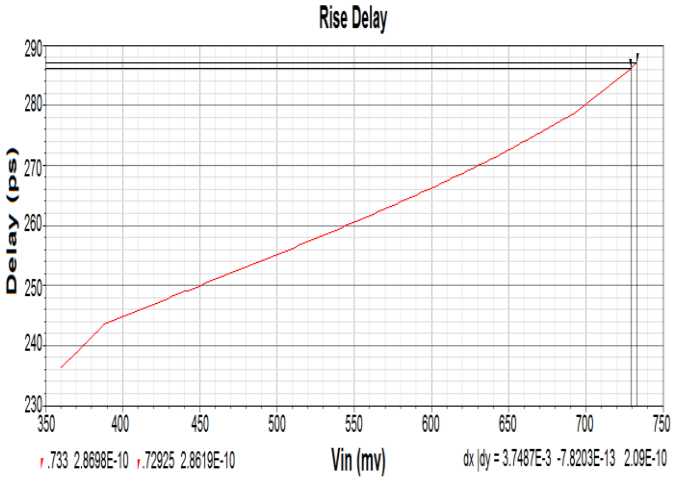

Fig. 12. The linear dynamic range of the ADC based on the VCDU Circuit with the voltage sensitivity calculation on Cadence.

For the ADC based on the VCDU circuit and the first proposed VTC architecture: the linear range of V_{IN} is from -187 *m*V to 187 *m*V and from -280 *m*V to 280 *m*V (i.e. the dynamic range (DR) is 374 *m*V and 560 *m*V), the sensitivity is 0.29 *p*s/*m*V and 0.91 *p*s/*m*V (shown in Fig. 12 and Fig. 13), respectively. Due to the fact that high frequencies distort the signal linearity, low frequencies applications can get higher dynamic range than that at high frequency. Table 1 and 2 show all specifications for both designs, in case of a 8 GHz F_S. Also, Table 2 shows the specifications for a low sampling frequency (i.e. a 1 GHz F_S). Fig. 14 and Fig. 15 show the linear range with curve fitting using MATLAB for both circuits, while Fig. 16 and Fig. 17 show the linearity error check.

Table 3: Performance Comparison between the Second Proposed ADC and the Single-Ended Approach @ 3% Error

Parameter	Falling circuit of this work	Rising circuit of this work	Proposed circuit of this work	Falling circuit of [7]	Rising circuit of [7]	Proposed circuit of [7]
DR (mV)	528	1136	1000	240	400	550
Sensitivity (ps/mV)	0.97	2.7	9.6	0.64	2.45	2.13
THD @ FS,MAX (dB)	-29.4069	-7.8186	-13.3057	-9.9	-12.45	-20
Power Dissipation @ FS/FS,MAX (µW)	19.41/259.1	15.7/37.2	159/358.2	9.65/-	9.138/-	61.86/-
FS,MAX (GHz)	4	0.7	2.5	1.6	0.285	0.7
DR @ FS,MAX (mV)	364	620	462	80	140	550
FOM1 @ FS/ FS,MAX (×1012)	3.59/2.05	20.5/7.23	1.57/1.49	1/-	0.14/-	3.4/-

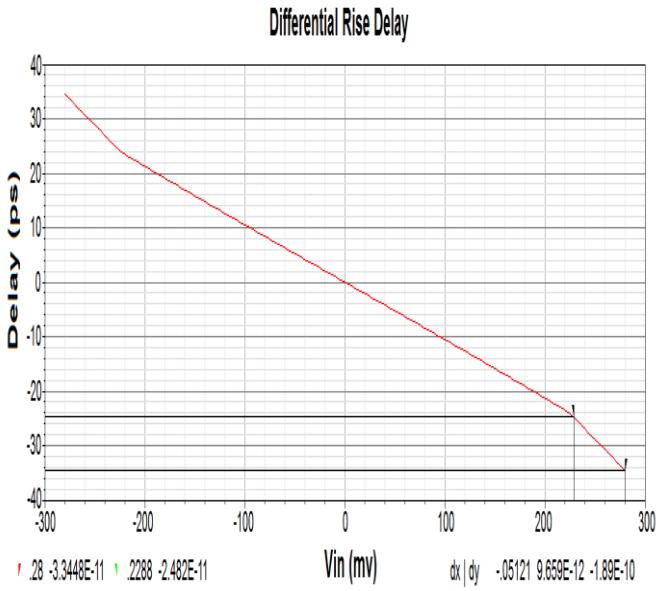

Fig. 13. The linear dynamic range of the first proposed ADC Circuit with the voltage sensitivity calculation on Cadence.

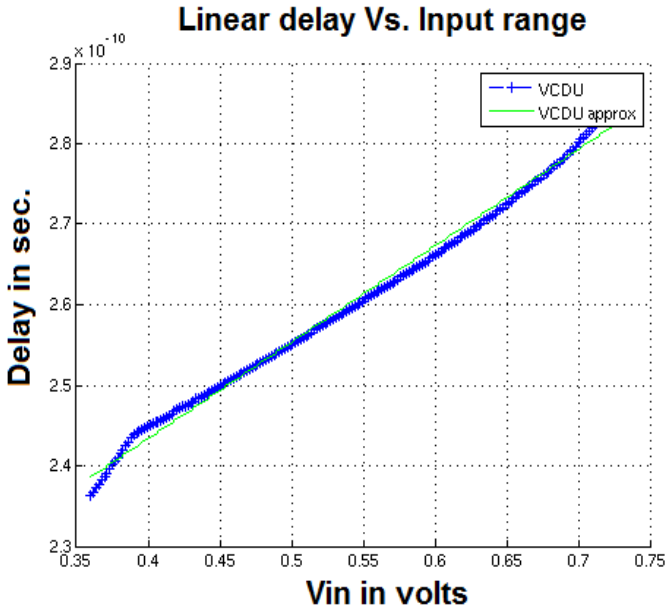

Fig. 14. Curve fitting using MATLAB for the linear range of the ADC based on the VCDU circuit

For the falling-differential VTC, rising-differential VTC and the second proposed ADC architecture circuits: the linear range of V_{IN} is from -264 *m*V to 264 *m*V, from -568 *m*V to 568 *m*V and from -500 *m*V to 500 *m*V (i.e. the dynamic range is 528 *m*V, 1136 *m*V and 1000 *m*V); the sensitivity is 0.97 *ps*/*m*V, 2.7 *ps*/*m*V and 9.6 *ps*/*m*V respectively (shown in Fig. 18(a), Fig. 18(b), Fig. 19(a), Fig. 19(b), Fig. 20(a) and Fig. 20(b) at sampling frequency (Fs) of 250 MHz).

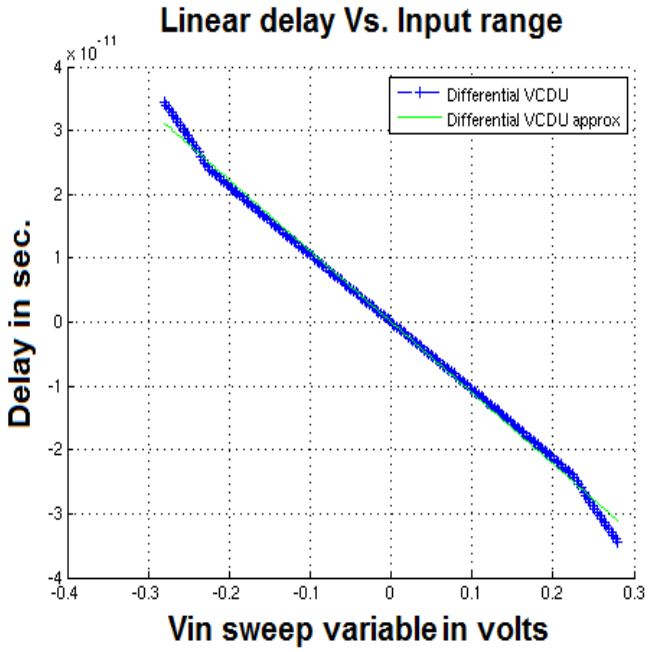

Fig. 15. Curve fitting using MATLAB for the linear range of the first proposed ADC circuit.

4.2 Maximum Sampling Frequency, Power Consumption

As the proposed designs have higher DR, we can increase the sampling frequency of each circuit. Due to the fact that increasing Fs distorts the signal linearity, we will reduce the dynamic range to keep the error below 3%. This procedure is permitted, as long as we have a higher dynamic ranges for all differential designs than single-ended designs. As the dominant power consumption in a CMOS circuit (i.e. A CMOS circuit has a very low static power consumption results from the flowing leakage current) is dynamic power when switching at a high frequency, dynamic power contributes significantly

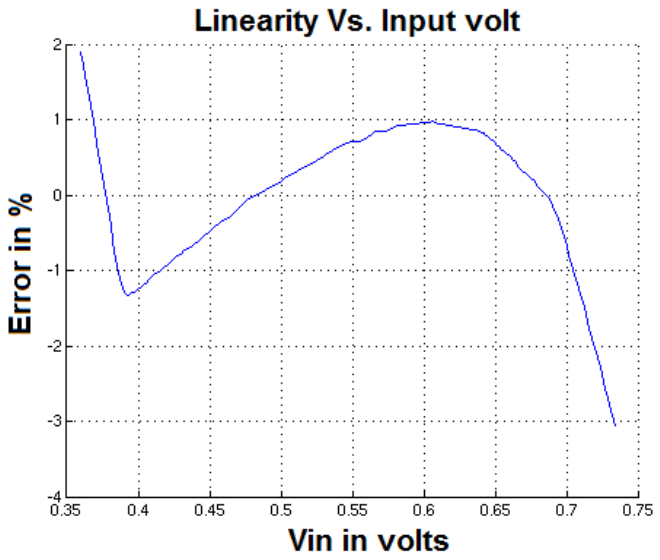

Fig. 16. Linearity error check using MATLAB for the linear range the ADC based on the VCDU circuit.

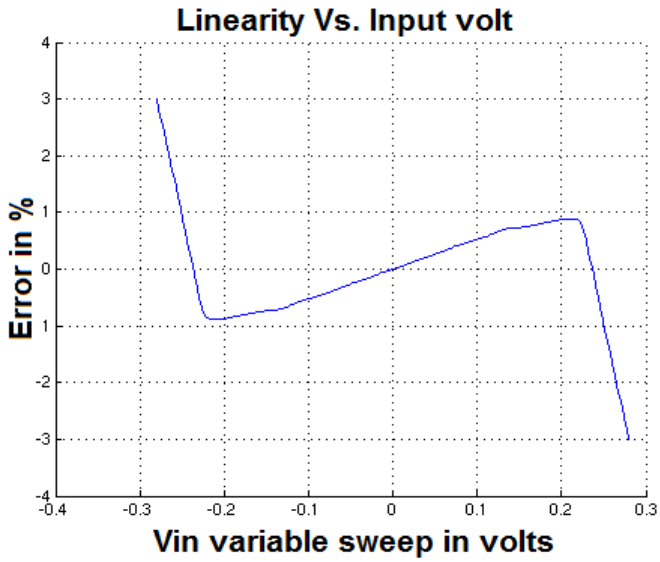

Fig. 17. Linearity error check using MATLAB for the linear range of the first proposed ADC circuit.

to the overall power consumption. Fig. 18(c), Fig. 18(d), Fig. 19(c), Fig. 19(d), Fig. 20(c) and Fig. 20(d) show the linear range with curve fitting and the linearity error check for each design at its maximum F_S.

Table 3 compares all the specifications, at a 3% acceptable dynamic range error, of the falling-differential VTC, the rising-differential VTC and the second proposed designs of this work and the corresponding single-stage designs of [7]. The differential rising-VTC circuit has the highest linear range, due to the small value of the parasitic capacitance of node VF in Fig. 9(a). This produces a low circuit speed. Hence, this differential rising-VTC has a lower Fs,max of 700MHz than other circuits.

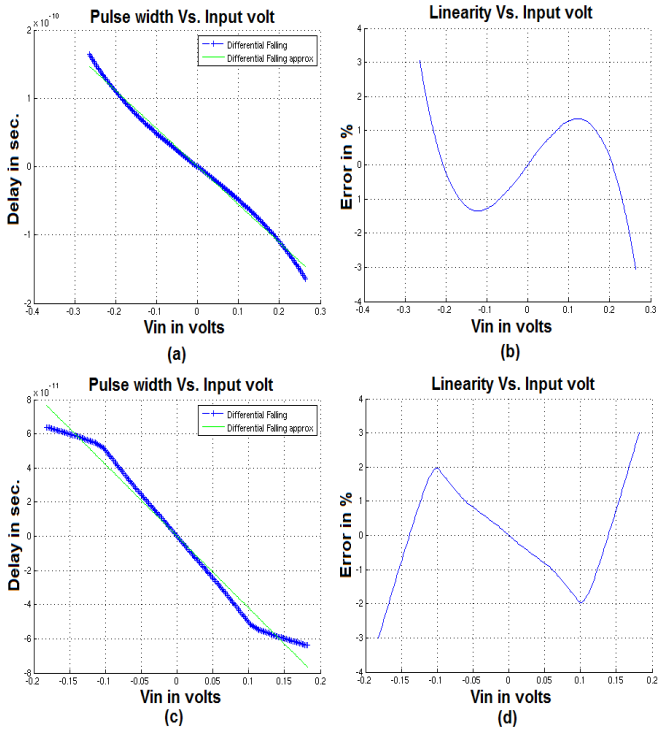

Fig. 18. Falling differential VTC. (a) Linear range at F_S =250MHz. (b) Linearity error check at Fs =250MHz. (c) Linear range at $F_{S,MAX}$ =4GHz. (d) Linearity error check at $F_{S,MAX}$ =4GHz.

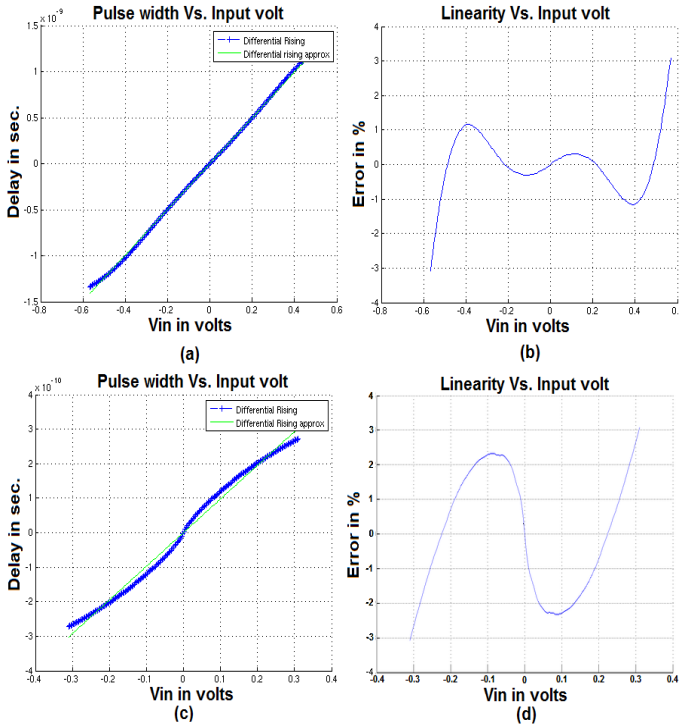

Fig. 19. Rising differential VTC. (a) Linear range at F_S =250MHz. (b) Linearity error check at Fs =250MHz. (c) Linear range at $F_{S,MAX}$ =700MHz. (d) Linearity error check at $F_{S,MAX}$ =700MHz.

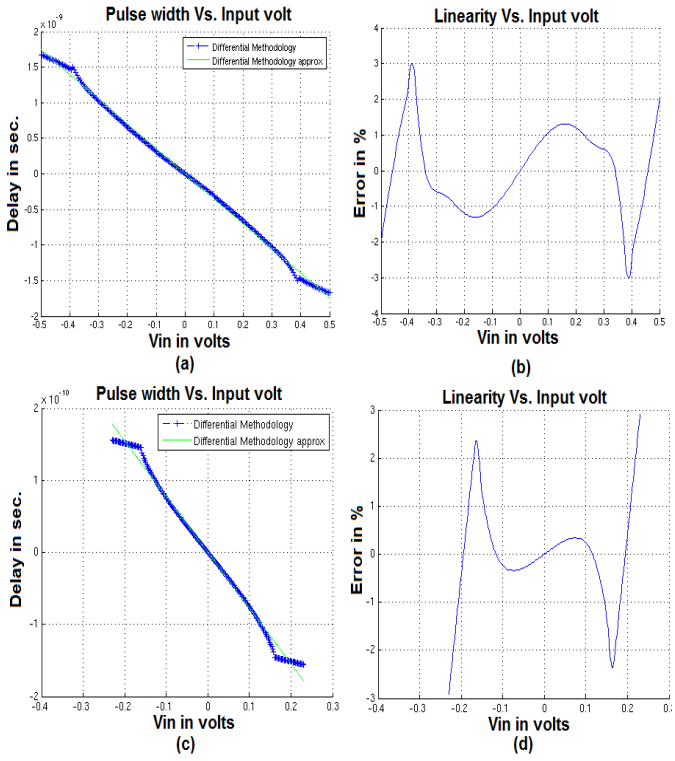

Fig. 20. The second proposed ADC. (a) Linear range at Fs =250MHz. (b) Linearity error check at F_S =250MHz. (c) Linear range at $F_{S,MAX}$ =2.5GHz. (d) Linearity error check at $F_{S,MAX}$ =2.5GHz.

4.3 Total Harmonic Distortion

The Total Harmonic Distortion (THD) is one of the main metrics for quantifying the circuit linearity. THD is a measure of the ratio of the square root between all the input signal harmonics RMS value ($V_{i,RMS}$) and just the harmonically-related distortion component (the fundamental frequency $V_{Fundamental,RMS}$) and is expressed in decibels as in equation (2). THD can be measured by replacing the DC Input Voltage with a sinusoidal waveform in all schematic designs. Due to a differential circuit nature, the amplitude of the waveform will be half of the dynamic range. Then the input frequency will be swept.

$$THD = 20\log\left(\sqrt{\left(\frac{\sum_{i\neq 1} V_{i,RMS}}{V_{fundamntal,RMS}}\right)}\right) \qquad (2)$$

Table 4 shows THD calculations over various input frequencies for the ADC based on VCDU design and the first proposed ADC architecture. We can notice that the linearity is improved in mid frequencies at the proposed architecture (i.e. starting from lower frequencies till frequencies less than 5 GHz). At high frequencies, the fundamental frequency (i.e. 8 GHz) is much greater than other harmonics by more than 25 dB. Thus, these ADCs produce a highly linear output closer to the analog input.

Table 4: THD Calculations in Case of 8 GHz FS

F_{IN} (GHz)	ADC Based on VCDU	The First Proposed ADC
3	-5.7504	-10.2322
5	-18.4887	-22.7074
8	-29.3727	-25.8196

Table 5, 6 and 7 show the THD calculations for the falling-differential VTC, the rising-differential VTC and the second proposed ADC respectively. At 250 MHz FS, the 1st design has highly harmonic components than the fundamental frequency.

Table 5: THD Calculations in Case of a Maximum FS of 4 GHz For the Falling-Differential ADC

F_{IN} (MHz)	The Falling-Differential ADC
0.1	-17.2852
500	-17.3152
1000	-17.9238
2000	-23.3544
4000	-29.4069

Table 6: THD Calculations in Case of a Minimum/Maximum FS For the Rising-Differential ADC

F_S = 250 MHz		$F_{S,MAX}$ = 700 MHz	
F_{IN} (MHz)	The Rising-Differential ADC	F_{IN} (MHz)	The Rising-Differential ADC
0.1	-14.913	0.1	-6.6329
50	-17.973	50	-6.8204
100	-17.4854	400	-15.339
250	-16.5394	700	-7.8186

Table 7: THD Calculations in Case of a Minimum/Maximum FS For the Second Proposed ADC

F_S = 250 MHz		$F_{S,MAX}$ = 2.5 GHz	
F_{IN} (MHz)	The Rising-Differential ADC	F_{IN} (GHz)	The Rising-Differential ADC
125	-1.7994	1	-10.6362
150	-3.3332	2	-12.7065
250	-6.0994	2.5	-13.3057

So, it is not good to operate on this frequency. While in a maximum F_S of 4 GHz, we notice that the linearity enhances till we reach an input frequency of 4 GHz (i.e. a THD of -29.4069). The compliment of the linearity takes place in the rising-differential VTC. So, the linearity enhances in low F_S of 250 MHz than in high F_S of 700 MHz.

On the other hand, for the second proposed ADC, the linearity is enhanced at high values of F_S close to 2.5 GHz than values close to 250 MHz. This proposed design has an improved THD than the rising-differential VTC and a quiet less THD than that of the falling-differential VTC, in case of high sampling frequencies. While at low sampling frequencies, it has a better THD than the 1st design and a quiet less THD than the 2nd one. This because the complimentary approach while designing the first 2 designs.

4.4 Effective Number of Bits

Effective Number of Bits (ENOB) is considered the main metric that tests all different types of errors (including distortion errors) that an ADC faces. To calculate the ENOB [12], we first measure the Signal-to-Noise-and-Distortion (SNDR) ratio as in equation (3) where $V_{IN,RMS}$, $V_{NOISE,RMS}$ and $V_{DISTIORTION,RMS}$ are the RMS value of the input voltage, the output voltage due to the existence of noise and the output voltage due to the circuit distortion and frequency harmonics respectively. Then we can substitute with the SNDR in equation (4) to get the ENOB with the help of the Fast Fourier Transform (FFT) technique [3]. The high accuracy of ENOB results depends on the larger FFT size.

$$SNDR = 20log(\frac{V_{IN,RMS}}{V_{NOISE,RMS}+V_{DISTORTION,RMS}}) \quad (3)$$

$$ENOB = \frac{SNDR+1.76}{6.02} \quad (4)$$

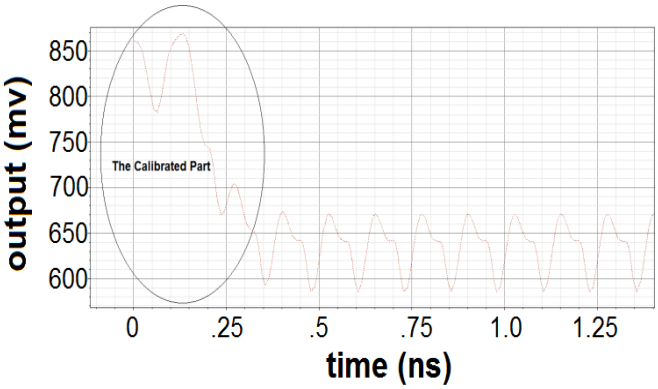

Fig. 21. Number of output samples of the ADC based on VCDU circuit.

For the ADC based on the VCDU and the first proposed ADC, the VCDU and the VTC output are shown in Fig. 21 and Fig. 22 with a highlighted calibrated part respectively. For a FFT size of 1024, we get a SNDR of 35.91 dB and an ENOB of 5.673 for the 6-bit ADC based on VCDU.

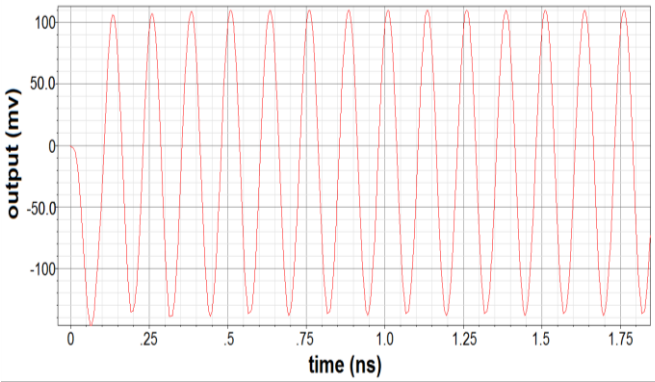

Fig. 22. Number of output samples of the first proposed ADC.

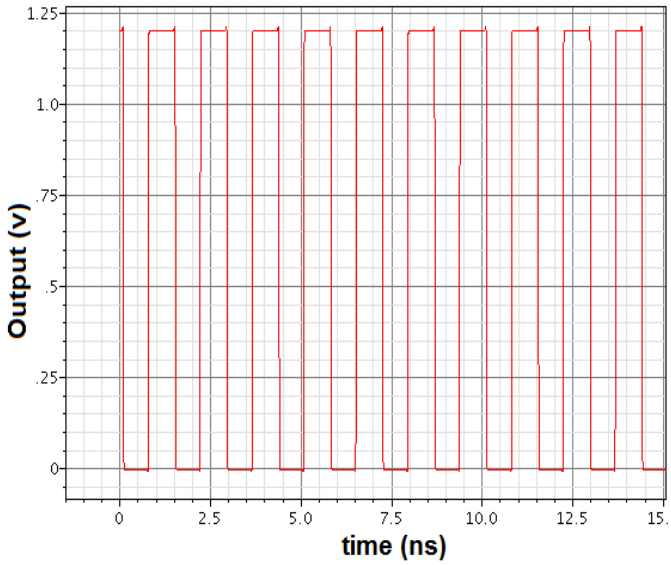

Fig. 23. Capture of output samples of a single-ended second proposed ADC.

For a FFT size of 1024, we get a SNDR of 35.91 dB and an ENOB of 5.673 for the 6-bit ADC based on VCDU. With the same FFT size, we get a SNDR of 55.8809 dB and an ENOB of 8.9902 for the first proposed ADC. ENOB results in both circuits reach the A ADC number of bits due to the very low THD (i.e. few errors).

A single-ended ADC based on the new methodology is designed for the single-ended VTC of [7] to reveal the performance of the second proposed ADC. The VTC output of both circuits is shown in Fig. 23 and Fig. 24 respectively. For a FFT size of 512, we get a SNDR of 48.8632 dB and an ENOB of 7.8245 for the 8-bit single-ended ADC based on the new methodology. With the same FFT size, the SNDR equals 66.3113 dB and the ENOB is 10.7228 for the 11-bit second proposed ADC.

4.5 Figure-of-Merit

In [13], R.H. Walden has discussed 2 approaches to calculate the Figure-of-Merit (FOM) as in equation (6) and (7). Where P and F_B are the power dissipation and the lower of either the effective resolution bandwidth or the Nyquist frequency. The FOM represents the efficiency of using the power to increase the DR and/or the maximum frequency.

FOM_1 is presented for the ADC based on VCDU, the first proposed ADC design and the second proposed ADC design in Table 1, 2 and 3 respectively.

Table 8: Comparison of 65-nm CMOS State-Of-The-Art ADCs @ 3% error

Parameter	This work	This work	[7]	[8]	[14]	[15]	[16]	[17]	[18]
Dynamic Range (*m*V)	560	1000	550	200	-	-	1Vpp	-	-
Sensitivity (ps/mV)	0.91	9.6	2.13	0.25	-	-	-	-	-
Resolution (bits)	9	11	-	4	5	5	4	6	6
ENOB at $F_{S,MAX}$ (bits)	8.9902	10.7228	-	3.5	4.4	4.04	3.01	5.02	4.94
SNDR Peak (dB)	55.8809	66.3113	-	22.9	28.248	26.1	19.9	32	31.5
Power Dissipation (mW)	1.594	0.159	0.06186	4	1.97	1.8	1.02	320	6.7
Maximum F_S (GHz)	8	2.5	0.7	7.5	0.8	0.5	1	5	1
FOM_1 ($\times 10^{12}$)/ FOM_2 (pJ/conv)	1.57/ 3.918$\times 10^{-4}$	1.57/ 3.763$\times 10^{-5}$	3.4/-	0.075/ 0.62	-/ 0.116	-/ 0.44	0.98/ 0.126	-/ 2	-/ 0.21

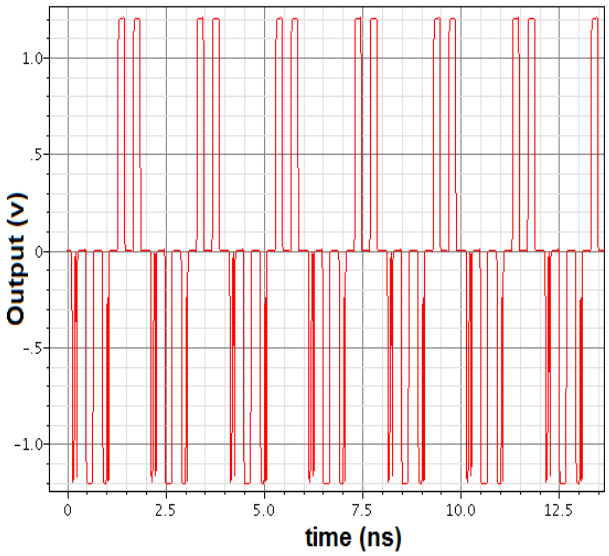

Fig. 24. Number of output samples of the second proposed ADC.

The proposed designs have small FOM_1 values due to the large power dissipation which under research to be minimized.
Table 8 compares the proposed 2 designs with all 65nm CMOS state-of-the-art ADCs which have discussed in [7], [8] and [14]–[18]. We can notice that, the first proposed ADC provides the highest dynamic range and sampling speed that the circuit can operate on and a reasonable sensitivity and the lowest FOM_2, in the expense of much power. On the other hand, the second proposed design provides the lowest FOM_2, the highest dynamic range, sensitivity and ENOB and a reasonable sampling speed.

$$FOM_1 = \frac{Fs \times DR^2}{P} \quad (5)$$

$$FOM_2 = \frac{P}{(2F_B) \times 2^{ENOB}} \quad (6)$$

5. Simulation Results

In this paper, 2 novel ADC circuits are proposed which achieve a higher operating sampling frequency, linearity, dynamic analog input range, sensitivity and ENOB with a lower FOM. The novelty in these designs is emerged from some reasons. First, this work depends on the differential mechanism, in which the even order harmonics are suppressed and the input voltage noise is discarded. Second, the power of CMOS technology which provides a high-speed and low-power design. Finally, for the second proposed design, we provide an output pulse width which is proportional to the analog input voltage, is the difference between the rising delay and the falling delay of 2 current starved VTCs.
The first proposed ADC circuit provides a 8 GS/s sampling speed, 560 *m*V dynamic-range, 0.91 *ps/m*V sensitivity, 8.9902 ENOB for a 9-bit ADC, 1.594 *m*W power, -25.8196 THD, 1.57×10^{12} FOM_1 and 0.3918 *f*J/conversion FOM_2. The second proposed ADC circuit provides a 2.5 GS/s sampling speed, 9.6 *ps/m*V sensitivity, 1000 *m*V dynamic-range, 10.7228 ENOB for a 11-bit ADC, 159 μW power, -13.3057 THD, 1.49×10^{12} FOM_1 at $F_{S,MAX}$ and 0.03763 *f*J/conversion FOM_2. This work does not depend on the existence of a sample-and-hold (S/H) circuit for analog input frequencies up to 8 GHz for the first design or frequencies up to 2.5 GHz for the second design. If higher input frequencies are expected, the S/H circuit is used.

References

[1] A. El-Bayoumi, H. Mostafa, and A.M. Soliman, Design of High-Performance Differential Voltage-to-Time Converters, Lambert Academic Publishing (LAP), Germany, 2016.
[2] A. El-Bayoumi, H. Mostafa, and A.M. Soliman, "A Novel MIM-Capacitor Based 1-GS/s 14-bit Variation-Tolerant Fully-Differential Voltage-to-Time Converter (VTC) Circuit," Journal of Circuits, Systems, and Computers (JCSC), vol. 26, no. 5, pp. 1-32, 2017.
[3] A. El-Bayoumi, H. Mostafa, and et al., "A New 65nm-CMOS 1V 8GS/s 9-bit Differential Voltage-Controlled Delay Unit Utilized for a Time-Based Analog-to-Digital Converter Circuit," 27th IEEE International Conference on Microelectronics (ICM), pp. 158-161, 2015.
[4] A. El-Bayoumi, H. Mostafa, and et al., "A New 16-Bit Low-Power PVT-Calibrated Time-Based Differential Analog-to-Digital Converter (ADC) Circuit in CMOS 65nm Technology," 22nd IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Egypt, pp. 492-493, 2015.
[5] Guansheng Li, Y.M. Tousi, A. Hassibi, and E. Afshari, "Delay-Line-Based Analog-to-Digital Converters," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 56, no. 6, pp. 464–468, 2009.

[6] A. El-Bayoumi, H. Mostafa, and A.M. Soliman, "A New Highly-Linear Highly-Sensitive Differential Voltage-to-Time Converter Circuit in CMOS 65nm Technology," 19th IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1262-1265, 2015.

[7] M.W. Ismail, and H. Mostafa, "A New Design Methodology for Voltage-to-Time Converters (VTCs) Circuits suitable for Time-Based Analog-to-Digital Converters (T-ADC)," 2014 27th IEEE International System On Chip Conference (SOCC), pp. 103–108, 2014.

[8] A.R. Macpherson, J.W. Haslett, and L. Belostotski, "A 5GS/s 4-bit Time-Based Single-Channel CMOS ADC for Radio Astronomy," 2013 IEEE Custom Integrated Circuits Conference (CICC), pp. 1–4, 2013.

[9] C.S. Taillefer, "Analog-to-Digital Conversion via Time-Mode Signal Processing", A thesis submitted to the Faculty of Graduate Studies and Research in McGill University in partial fulfillment of the requirements for the degree of Doctorate of Philosophy, May 2007.

[10] C.S. Taillefer, and G.W. Roberts, "Delta–Sigma A/D Conversion Via Time-Mode Signal Processing," IEEE Transactions on Circuits and Tim-
e-Mode Signal Processing," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 56, no. 9, pp. 1908–1920, 2009.

[11] B.A. Minch, "Low-Voltage Wilson Current Mirrors in CMOS," IEEE International Symposium on Circuits and Systems (ISCAS07), pp. 2220–2223, May 2007.

[12] S. Weaver, B. Hershberg, and Un-Ku Moon, "ENOB Calculation for ADCs with Input-Correlated Quantization Error Using a Sine-Wave Test," 22nd International Conference on Microelectronics (ICM 2010), pp. 5–8, 2010.

[13] R.H. Walden, "Analog to Digital Converter Survey and Analysis," IEEE Journal on Selected Areas in Communications, vol. 17, no. 4, pp. 539–550, 1999.

[14] Y. Lin, S. Chang, Y. Liu, C. Liu, and G. Huang, "A 5b 800MS/s 2mW asynchronous binary-search ADC in 65nm CMOS," IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, pp. 80–81, Feb. 2009.

[15] B.P. Ginsburg, and A.P. Chandrakasan, "500-MS/s 5-bit ADC in 65nm CMOS with split capacitor array," IEEE Journal of Solid-State Circuits, vol. 42, no. 4, pp. 739–747, Apr. 2007.

[16] Y.M. Tousi, Guansheng Li, A. Hassibi, and E. Afshari, "A 1mW 4b 1GS/s Delay-Line based Analog-to-Digital Converter," ISCAS09, pp. 1121–1124, May 2009.

[17] M. Choi, Jungeun Lee, Jungho Lee, and Hongrak Son, "A 6-bit 5-GSample/s Nyquist A/D converter in 65nm CMOS," 2008 IEEE Symposium on VLSI Circuits, pp. 16–17, 2008.

[18] Jing Yang, T.L. Naing, and B. Brodersen, "A 1-GS/s 6-bit 6.7-mW ADC in 65-nm CMOS," IEEE 2009 Custom Intergrated Circuits Conference (CICC), pp. 287–290, 2009.

Biography

Abdullah El-Bayoumi received the B.Sc. and M.Sc. in Electronics Engineering from Cairo University, Egypt in 2012 and 2016 respectively. He has worked as an Embedded Systems Engineer in the ESP (Egyptian Space Program) at NARSS (National Authority for Remote Sensing and Space Sciences), Egypt for 2 years. He has been working at Valeo Egypt as Senior Software Engineer since 2015. He has authored over 9 papers in international journals and conferences and is the author of the books: "LTE-A Filter and Variable Gain Amplifier Blocks (LAP LAMBERT, Germany, 2016" and "Design of High-Performance Differential Voltage-to-Time Converters (LAP LAMBERT, Germany, 2016". His research interests include analog/mixed signal design, embedded systems design and low-power RF transceivers design.